## ABSTRACT OF THE DISCLOSURE

The present invention is directed to a system and method for implementing a pre-steered instruction cache. The hardware logic that normally steers instructions to specific execution units just prior to execution is moved before the pre-steered instruction cache, so that instructions are pre-steered into that cache. This is done so that an instruction can leave the pre-steered instruction cache and enter the execution unit that can execute it with either minimum or no steering logic involvement. The cache lines of the pre-steered instruction cache are organized into bins such that each bin corresponds to either a single execution unit or a cluster of execution units.